

KIRTHANA P RAO

Email: work.kirthana@gmail.com | Place: Bangalore, India

+91 94970-24531

[LinkedIn](#) | [GitHub](#)

PROFESSIONAL SUMMARY

Motivated and detail-oriented ECE graduate seeking a challenging role in Systems Design & Verification. Dedicated to continuous learning and eager to research and contribute, with keen interest in Embedded Systems and at the intersection of AI and VLSI, with interests in Cybersecurity, Healthcare Technology and Sustainable Manufacturing.

TECHNICAL SKILLS

- **Languages:** C, C++, Python, Verilog HDL, TL-Verilog HDL
- **Hardware Tools:** Cadence Virtuoso, Xilinx Vivado, ModelSim, KiCAD, MATLAB Simulink, OpenLANE, OpenSTA, Keil, LTSpice
- **Platforms & Frameworks:** RISC-V ISA, Linux OS, AXI4-Stream/AXI-4 Lite Protocol, Arduino IDE, TensorFlow 2.0, ONNX, FINN Compiler
- **Core Concepts:** Digital Design, Machine Learning, Agile Methodologies, Data Structures & OOP, Timing Analysis, PCB Design

EDUCATION

Indian Institute of Information Technology, Design & Manufacturing, (IIITDM) Kurnool

B.Tech Electronics & Communication Engineering with Specialization in Design and Manufacturing

Nov 2022 – Jul 2026

Christ Academy CBSE School

Intermediate (XI-XII) · Physics, Chemistry, Mathematics, Computer Science

Jun 2020 – Jul 2022

EXPERIENCE

Research Intern, Indian Institute of Science (IISc), Bangalore

Worked on development of end-to-end implementation framework for ML algorithms for deploying on FPGAs, with Models like Lenet-5 and BERT Transformer, using the ONNX to RTL flow at Future Computing Systems (FIST) Lab, Dept. of Computer Science and Automation.

Jan 2026 – Jul 2026

Summer Intern on 'Digital Systems Prototyping using FPGAs' – NIELIT Calicut, Kozhikode

Completed an intensive training in RTL Design and FPGA-based logic synthesis, and performed RTL coding, testbench development, and synthesis workflows for FPGA implementations, to create and verify the designs meeting performance and functional requirements.

May 2025 – Jun 2025

Research Intern, TiHAN – IIT Hyderabad, Hyderabad

Developed a Machine Learning Model for use-case in an ADAS-based Project, which secured over 94% accuracy, and as Project Intern on Network Handover between Cellular Networks (4G LTE) and Wi-Fi Network, using Bash and OpenAir Interface in Unix CLI, at the Connected Autonomous Vehicles (CAV) Lab.

Jun 2024 – Jul 2024

PROJECTS

Hardware Implementation of Number Theoretic Transforms (NTT)

RTL Implementation of NTT is performed using Verilog HDL followed by designing a verification environment for a small-scale NTT and INTT architecture.

Jun 2026 – Present

- **Key Skills:** Modular Arithmetic Units · RTL Design · Verilog

Design of Compressor Based Dadda Multiplier

Designed and implemented 4-2 and 3-2 compressors for large-scale multiplier applications- an 8x8 bit Dadda Multiplier, in Xilinx Vivado 2024.2v. Resulted in the power reduction by about 8%, and better utilization of area.

Mar 2025 – Apr 2025

- **Key Skills:** RTL Design · Verilog · Digital Logic Design

Design and Simulation of RISC-V ALU and a Pipelined RISC-V Processor

Created a robust implementation of a multi-stage pipelined RISC-V processor emulator featuring comprehensive hazard detection and resolution mechanisms. Designed and debugged a single-cycle RISC-V ISA implementation using GCC compilation and Spike simulator validation, covering instruction decoding, register file management, ALU operations, and control flow hazard mitigation.

May 2025

- **Key Skills:** TL-Verilog · C · RISC-V · Verilog

CERTIFICATIONS

- Digital Design with Verilog, NPTEL and C-Based VLSI Design, NPTEL by IIT Guwahati
- VLSI Design Flow: RTL to GDS, NPTEL by IIIT Delhi
- Machine Learning Specialization by Stanford University & DeepLearning.AI on Coursera
- Neural Networks and Deep Learning and Convolutional Neural Networks by DeepLearning.AI on Coursera
- Minor Degree in Internet of Things (IoT), IIITDM Kurnool

ACHIEVEMENTS

- Ranked among the top 0.1% of Computer Science students in the CBSE Secondary School Examination 2022.
- Second runner-up as a team in RoboRhythm competition - in building a Line Following Robot (LFR) in SOLASTA Techno-Cultural Fest 2K24
- ISWDP Samsung Student Fellowship Recipient

LANGUAGES KNOWN

English, Hindi, Kannada, Malayalam, Konkani, Telugu

EXTRA CURRICULAR

Technical Coordinator at *ElectroniX Club*, IIITDM Kurnool · *Roohaniyat Music Club*, IIITDM Kurnool

Carnatic Vocal Music – Passed with *First Division* in Vocal Music by *Bangiya Sangeet Parishad*

2018

Orator and Emcee